REMARKS

Claims 1 and 3-19, as amended, appear in this application for the Examiner's review and consideration. Claim 1 has been amended to recite that the wafer surface is treated prior to polishing to increase surface roughness, and claim 6 has been amended to be consistent with amended claim 1. Claims 5 and 15 have been re-written in independent form. Claims 17 and 19 have been amended to correct inadvertent errors in referring back to prior claims. New claims 20 recites the preferred surface roughness values that are achieved. The amendment to claim 1 and the features of claim 20 are supported in the specification at page 3. As no new matter has been introduced by these changes or additions, they all should be entered at this time.

Claims 1, 4, 10-14 and 17 were rejected under 35 USC 103(a) as being unpatentable over the combination of US patents 5,895,583 to Augustine et al. ("Augustine ") and 6,136,727 to Ueno et al. ("Ueno") with Japanese patent application 07-288243 to Ogino et al. ("Ogino") for the reasons set forth on pages 3-5 of the action. Also, claims 3, 16, and 18-19 were rejected over the previous combination of references with the addition of US patent 5,877,070 to Gosele and claims 6-9 were rejected over the previous combination of references with the addition of US patent 6,833,562 to Tanimoto et al. ("Tanimoto") for the reasons set forth on pages 5-7 of the action.

Before addressing these rejections, a brief review of the presently claimed invention may be helpful. The invention as defined by current claim 1 relates to a method of preparing a wafer surface to make it ready for further epitaxial growth. The method includes an annealing step followed by treatment and polishing steps. In particular, the annealing step is an oxidation step, the treatment step is preferably a deoxidation step and a chemical mechanical polishing ("CMP") step using colloidal silica. These treatments provide a wafer surface that is ready for epitaxy (i.e., it is "epiready" as described) on thin SiC films, using a rapid technique, which employs steps and machines that are standard in microelectronics. The smoother the final SiC surface and the lower its roughness, the better the quality of the epitaxy, with the yield of electronic components produced on the thin film substantially increased. The method of the invention thus produces a good quality surface that is not rough and is sufficiently smooth to be used for producing good quality homoepitaxy (SiC on SiC epitaxy), as well as heteroepitaxy (AlN, AlGaN or GaN on SiC) thereon. The invention is useful for treating polytype 4H SiC substrates as well as other SiC substrates, such as a polytype 6H or 3C SiC substrates.

Turning now to the cited references, Augustine discloses silicon carbide wafers prepared for semiconductor epitaxial growth by first lapping a silicon carbide wafer derived from a boule, placing the wafer in a recess of a metal backed template and moving the wafer over and against a rotating plate. Two different diamond slurry mixtures of progressively smaller diamond grit sizes are sequentially used, along with a lubricant, for a predetermined period of time. The lapping operation is followed by a polishing operation which sequentially utilizes two different diamond slurry mixtures of progressively smaller diamond grit sizes, along with three different apertured pads sequentially applied to a rotatable plate, with the pads being of progressively softer composition. The wafers may cleaned and the templates changed after each new diamond slurry mixture is used.

The Examiner's characterization of Augustine is essentially correct. Applicants discuss this patent in the specification on page 2: Augustine discloses CMP of SiC in successive steps, with a multiplicity of slurry mixtures of smaller size. A good description of the problem that is solved by the present invention is presented in Augustine in column 1, lines 33-51. Namely, the sawing operation conducted on a silicon carbide crystal boule results in a wafer surface which, although appearing smooth, actually is damaged and contains microscopic scratches completely unacceptable for a subsequent epitaxial growth procedures. Due to this damaged surface, the resulting semiconductor device would either not operate or operate at reduced efficiency. To remedy this, the surface must be highly polished to substantially eliminate all traces of any scratches and surface defects. In view of the fact that silicon carbide is twice as hard as silicon, the exact process for polishing silicon wafers is unsuitable for silicon carbide. Conventional optical polishing techniques may take ten days or more to achieve an acceptable surface finish for silicon carbide wafers.

Augustine's solution to the problem is to polish the wafer surface for up to 3 hours of polishing time using different types of slurries. This complex and time consuming operation is not useful in a commercial setting as it is too slow and cumbersome to facilitate efficient manufacturing or production. The Examiner has noted that Augustine does not teach or utilize an annealing step condition the wafer surface, and this is claimed in the present invention. The use of the annealing step, in combination with the subsequent treatment step, reduces the polishing time to between about 15 to 30 minutes using a single type of slurry based on colloidal silica. This is a significant

improvement over Augustine as colloidal silica is less expensive and easier to use compared to diamond abrasives.

Thus, the Ueno patent is cited in an attempt to remedy the deficiencies of Augustine. The motivation for combining these references is stated as being the implementing of oxidation to increase the value of channel mobility. Applicants traverse the rejection, since even if channel mobility is increased, this does not teach the skilled artisan how to reduce the preparation time of obtaining a good quality wafer surface that is not rough and is sufficiently smooth to be used for producing good quality epitaxy thereon.

Ueno discloses a method for forming a thermal oxide film of a silicon carbide semiconductor device wherein the method includes a preliminary treatment in which a silicon carbide substrate is heated to 800 to 1200°C in an atmosphere comprising hydrogen or a mixture of hydrogen and inert gas, and then a silicon dioxide film is formed on the substrate by thermal oxidation.

Ueno specifically teaches that oxidation of SiC to form a SiO2 layer on a SiC substrate leads to an interface of SiO2/SiC having degraded electrical performance (DIT, see column 2, line 53-62). The solution provided by Ueno to solve this problem consists in having an additional hydrogen anneal step before the oxidation step (see column 3, line 3-15). In Ueno, the objective is to form a gate oxide layer, that is an oxide layer used in the final semiconductor device and that must have excellent electrical characteristics. Actually, Ueno is directed to a very different technical field compared to the present invention, namely, the formation of microelectronic devices compared to wafer surface preparation. Ueno is not trying to form or provide an epiready surface but instead is trying to increase interface trap density (DIT, an important electrical characteristics when forming devices) of a SiC/SiO2 interface, and an increase in channel mobility in such devices. Thus, Ueno is non-analogous art and should not be combined with Augustine as suggested in the office action.

Furthermore, even if combined, the references do not teach the presently claimed method. Augustine uses diamond particles whereas the present process enables the applicants to use colloidal silica particles in the polishing step. Also, Ueno uses SiO2, a material commonly used for forming gate dielectric in MOS semiconductor devices, as the oxide layer that is part of the final device. That oxide surface is not treated as recited in current claim 1 to increase its roughness, nor is it subject to a deoxidizing step or an RCA (SC1, SC2) type chemical cleaning (claims 6-7), chemical cleaning (claims 8-9) or

etching (claim 15) as these steps would remove a portion of the oxide layer, thus contradicting Ueno's reason for using the oxide in the first place.

To the extent that the office action is suggesting that Ueno's oxidation process leads to better surface characteristics, applicants also traverse that suggestion. It is clear that Ueno uses the additional hydrogen annealing step rather than the oxidation step to achieve the improved electrical characteristics. It is also clear that the improvement is electrical in nature and not related to surface preparation (roughness) for further epitaxial deposition of for any other reason relating to surface treatment. As noted above, the oxidation step in Ueno is used to create a layer of SiO2 and form a gate oxide layer that has an interface with the underlying SiC with the goal of improving the electrical characteristics of this interface which had been observed as usually being bad.

To summarize, Augustine and Ueno relate to complete different fields and should not be combined as suggested. There is nothing in Augustine that would suggest including an oxidation step before CMP, while Ueno's use of an oxide layer is an element of a device that does not improve surface characteristics of the substrate. Similarly, nothing in Ueno would suggest adding a CMP step that would lead to removal of the oxide layer as that layer is necessary for achieving the enhanced electrical properties of his devices. The improvement in channel mobility to justify the combination of these patents has no technical meaning: there is no channel on the surface SiC layer disclosed in the present invention. In addition, the improved mobility observe by Ueno is related to the prior hydrogen annealing step, and not to the oxidation step. Finally, neither reference teaches the use of colloidal silica as a suitable abrasive for us in the presently claimed polishing step.

Ogino is cited as a reference which teaches that colloidal silica is a suitable abrasive for treating silicon carbide surfaces. Applicants traverse this statement. Ogino discloses silicon oxide as one of three possible abrasives, but this is not colloidal silicon as claimed. Sometimes referred to as a sol or silica sol, colloidal silica is a stable dispersion of amorphous silica particles. To achieve this dispersion, the silica particles must be small enough such that they are largely unaffected by gravity. Therefore, silica particle sizes are usually of the order of less than 100 nanometers. The term "colloid" refers to the suspension, where the sols are the tiny discrete particles in suspension. Colloidal silicas can be manufactured from materials such as sodium silicate and are usually available in varying concentrations to suit various applications. None of this disclosure, nor even the use of the term "colloidal silica" appears in Ogino. Thus, a

skilled artisan would not look to Ogino as a teaching of the use of colloidal silica. Furthermore, Ogino would not be looked to for alternative abrasives for polishing silicon carbide since Augustine expressly teaches that hard diamond abrasives of different sizes must be used. As Augustine was filed after Ogino, Augustine certainly would have mentioned the abrasives disclosed in Ogino if such were useful in his process, but no such mention is made. Of equal importance, Ogino does not disclose the presently claimed annealing and treating process steps, and these are the steps that allow applicants' process to utilize colloidal silica rather than the diamond abrasives taught by the prior art in general and by Augustine in particular.

For the preceding reasons, the references that are combined to formulate the obviousness rejection of claim 1 are not related and do not provide the necessary motivation for the skilled artisan to combine them in an attempt to find the present invention obvious. Instead, this rejection has been formulated in hindsight utilizing the present specification and claims as a guide, a procedure which has been prohibited on many occasions by the Court of Appeals for the Federal Circuit. Accordingly, the obviousness rejection based on the combination of Augustine, Ueno and Ogino has been overcome as there is no incentive or motivation for the skilled artisan to combine these disclosures as suggested. Thus, this rejection should be withdrawn.

The secondary references to Gosele and Tanimoto do not remedy the deficiencies of the combination of Augustine, Ueno and Ogino to render obvious current claim 1.

Gosele discloses a method for transferring of monocrystalline, thin layers from a first monocrystalline substrate onto a second substrate, which may have a substantially different coefficient of thermal expansion than the first substrate is realized by producing hydrogen-traps in the first substrate by a first implantation and then implanting hydrogen followed by a heat-treatment to weaken the connection between the implanted layer and the rest of the first substrate, then forming a strong bond between the implanted first substrate and the second substrate and finally using another heat-treatment in order to split the monocrystalline thin layer from the rest of the first substrate by the formation, growth and overlapping of hydrogen filled microcracks. In the case of substrates with different thermal expansion coefficients the heat-treatment for splitting must be and can be at a temperature lower than a critical temperature at which the bonded pair degrades due to the mechanical stresses caused by the different expansion coefficients of the bonded-pair structure. Thus, Gosele does not produce a surface for

epitaxy, but instead transfers a thin layer from a donor wafer to a substrate. In addition to not teaching the method of claim 1, Gosele does not disclose what is claimed in claims 16 and 18-19.

Tanimoto discloses a silicon carbide semiconductor device and manufacturing method therefor, a metal electrode which is another than a gate electrode and which is contacted with a single crystalline silicon carbide substrate is treated with a predetermined heat process at a temperature which is lower than a thermal oxidization temperature by which a gate insulating film is formed and is sufficient to carry out a contact annealing between the single crystalline silicon carbide substrate and a metal after a whole surrounding of the gate insulating film is enclosed with the single crystalline silicon carbide substrate, a field insulating film, and the gate electrode. The present invention is applicable to a MOS capacitor, an n channel planar power MOSFET, and an n channel planar power IGBT. Like Ueno, Tanimoto is concerned with the preparation of electronic devices, rather than the surface preparation of a wafer for epitaxy. Again, Tanimoto does not disclose the process steps of claim 1 so that the fact that silicon substrates of electronic devices can be cleaned with hydrofluoric acid does not render obvious the invention of claims 6-9.

In view of the above, the entire application is believed to be in condition for allowance, early notice of which would be appreciated. Should any issues remain, a personal or telephonic interview is respectfully requested to discuss the same in order to expedite the allowance of all the claims in this application.

Respectfully submitted,

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